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EXAMINER	
MANDEVILLE, JASON M	

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2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/568,449	AYEL ET AL.	
	Examiner	Art Unit	
	JASON M. MANDEVILLE	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-28 and 30-37* is/are rejected.

7)☒ Claim(s) *19,21,27,29 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 February 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "simple memory" and the associated driving scheme as recited in **Claims 30 and 34** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. **Claim 21** is objected to because of the following informalities: the claim depends from itself. The examiner assumes, for the purposes of examination, that **Claim 21** is intended to depend from **Claim 20**. Appropriate correction is required.

3. **Claim 29** is objected to because of the following informalities: the claim does not exist. The claim numbering jumps from **Claim 28** to **Claim 30**. Appropriate correction is required.

4. **Claims 19, 21, 27, and 32** are objected to because of the following informalities: the claims contain inconsistent language, antecedent basis issues, and/or typographical errors. (In general, the claims are replete with inconsistent language, antecedent basis issues, and/or typographical errors; however, the above mentioned claims highlight those that are most readily identifiable). **Claim 19** recites "the capacitor" in the fourth line of the claim. The examiner assumes that "the capacitor" is meant to recite "the storage capacitor." **Claim 21** recites "the analogue DC voltage representing the gray level." The examiner assumes that the claim is meant to recite "the analogue DC voltage corresponding to the desired gray level" as was previously recited in **Claim 19**.

Claim 27 and **Claim 32** have stray parentheses in the third line of the claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claims 21-28 and 30-37** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims are replete with antecedent basis issues and inconsistent language making the claims vague, ambiguous, and all together unclear.

Claim 21 recites the limitation "the same threshold voltage value VT" in the last line of the claim. It is unclear whether "the same threshold voltage value VT" corresponds to the "switch-on threshold voltage VT" of **Claim 20**, or some other "same" threshold voltage value. The examiner contends that, if the "same threshold voltage value VT" refers to the "switch-on threshold voltage VT" of **Claim 20**, the word "same" is both superfluous and misleading, and should be removed for clarity.

Claim 22 recites "a supply voltage Vdd" as well as some undefined voltage quantity "Vi." It is unclear whether the "supply voltage Vdd" refers to the "a source voltage Vdd" of **Claim 19**, or some other voltage. The voltage value "Vi" is all together

undefined. Further, the wording of the claim is ambiguous and it is unclear what the voltage values Vi/VT or (VT-Vi)/VT is meant to define (i.e., the supply voltage Vdd or the fraction of a frame duration).

Claim 23 does not appear to add any further limitations to the method of **Claim 19**. **Claim 23** appears to be directed to "a ramp generator" (i.e., an apparatus) and does not add any method steps to the method of **Claim 19**. Further, **Claim 23** recites "a storage capacitor of each of the dots of the row." The "storage capacitor" is already defined in **Claim 19** as pertaining to an elementary liquid crystal cell and "the dots of the row" are all together undefined (i.e., there is not antecedent basis for these limitations).

Claim 24 recites "two storage capacitors and two transistors are associated with each elementary liquid crystal cell... the first capacitor... the first transistor... the second capacitor... the second transistor... the even frames... and... a linear ramp...." This claim is written as though it relates to an entirely different invention from the invention of **Claim 19**, making **Claim 24** (as well as **Claim 19**) wholly ambiguous and unclear. A "storage capacitor" is defined in **Claim 19** as being "associated with an elementary liquid crystal cell." **Claim 24** appears to define two additional "storage capacitors" and two additional "transistors." (Alternately, **Claim 24** could be defining one additional "storage capacitor" to be used, in some unclear way, in conjunction with the "storage capacitor" of **Claim 19**). As such, it is all together unclear how "the first capacitor," "the first transistor," "the second capacitor," and "the second transistor" fit into the framework of **Claim 19**. Furthermore, **Claim 24** again seems to be imparting apparatus limitations

into a method claim. In any case, **Claim 24** does not provide a clear understanding of the subject matter being claimed. The examiner suggests that if a structural relationship is being claimed, then that structure should be clearly recited in the claims. Furthermore, the "even frames" described by the claim and the receiving of "a linear ramp" appear to be the only limitations relating to method steps, and these steps are ambiguous and unclear as a "ramp" is previously defined and the "even frames" are not defined at all in the context of **Claim 19**.

Claim 25 recites the limitations "linked to the gate of the transistor" in the middle of the claim. There is not antecedent basis for this limitation in the claims and this feature seems to be essential to an understanding of the invention. Further, the claim is written as "the elementary circuit comprising: a storage capacitor... in series between to voltage supply terminals... the peripheral circuits...." However, as stated earlier in the claim, the "peripheral circuits" are not a part of the "elementary circuit" which makes the claim unclear.

Claim 26 recites the limitation "the transistor." It is unclear what "transistor" this limitations refers to.

Claims 27 and 32 recite "double memory comprising two storage capacitors and two switching transistors linked to the same elementary cell." These claims are written as though they relate to an entirely different invention from the invention of **Claim 25**, making **Claims 27 and 32** (as well as **Claim 25**) wholly ambiguous and unclear. A "storage capacitor" is defined in **Claim 25** as being associated with "an elementary liquid crystal cell." **Claims 27 and 32** appear to define two additional "storage

capacitors" in a "double memory" and two additional "switching transistors." (Alternately, **Claims 27 and 32** could be defining one additional "storage capacitor" to be used, in some unclear way, in conjunction with the "storage capacitor" of **Claim 25**). As such, it is all together unclear how "the first capacitor," "the first transistor," "the second capacitor," and "the second transistor" fit into the framework of **Claim 25**. In any case, **Claims 27 and 32** do not provide a clear understanding of the subject matter being claimed. The examiner suggests that the structural relationship defining the components in the invention should be clearly recited in the claims. Furthermore, the "even frames" and the "odd frames" described by the claim, and their relationship to the driving of the display are ambiguous and unclear. Further still, there are numerous uses of "the transistor" in the claim, none of which are clearly relatable to a single previously described element.

Claims 28 and 33 recites the limitation "all of the first capacitor." It is unclear what "capacitors" this limitations refers to.

Claims 30 and 34 recite a "simple memory with a single storage capacitor and a single switching transistor." These claims are written as though they relate to yet another entirely different invention from the invention of **Claims 25, 27, and 32**, making **Claims 30 and 34** (as well as **Claims 25, 27, and 32**) wholly ambiguous and unclear. Adding further to this ambiguity is the fact that there is no drawing illustrating the limitations of **Claims 30 and 34** (see the above objections to the drawings). A "storage capacitor" is defined in **Claim 25** as being associated with "an elementary liquid crystal cell." **Claims 30 and 34** appear to define an additional "storage capacitor" in a "simple

memory" and an additional "switching transistor." (Alternately, **Claims 30 and 34** could be defining some relationship between the previously defined "storage capacitor" and "storage capacitor" of **Claim 25**. If this is the case, these claims are at odds with **Claims 27 and 32**, or define a distinct invention as compared with **Claims 27 and 32**). As such, it is all together unclear how "the capacitor" and "the transistor" fit into the framework of **Claim 25**. In any case, **Claims 30 and 34** do not provide a clear understanding of the subject matter being claimed. The examiner suggests that the structural relationship defining the components in the invention should be clearly recited in the claims.

Claims 31 and 35-37 are rejected as being dependent from a rejected base claim.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. **Claims 19-28 and 30-37** are rejected under 35 U.S.C. 102(b) as being anticipated by Blalock et al. (hereinafter "Blalock" US 6,249,269).

9. As pertaining to **Claim 19**, Blalock discloses (see Fig. 4A, Fig. 8, and Fig. 7D) A method of controlling pixels of a liquid crystal display matrix (102; see Col. 1, Ln. 31-39; Col. 6, Ln. 38-60; and Col. 8, Ln. 11-46), comprising:

applying to a storage capacitor (160), associated with an elementary liquid crystal cell (118), an analog DC voltage (150) corresponding to a desired gray level (see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65),

linking a first terminal (159) of the capacitor (160) to the gate of a transistor (172) whose source is then linked to a ground (i.e., (V-), for example) and whose drain is linked to an electrode of the cell (118) and is also linked to a voltage source Vdd (i.e., (V+, Illum, or Bal), for example) across a current source (i.e., (170, 176, or 178), for example; again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65), and

applying to a second terminal (161) of the storage capacitor (160) a DC voltage ramp (Ramp) varying monotonically for the duration of an image frame (see Fig. 7D and again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65).

10. As pertaining to **Claim 20**, Blalock discloses (see Fig. 7D) that the voltage ramp (Ramp) varies in an essentially linear manner between a zero voltage level (i.e., 0V)

and a voltage level substantially equal to the value of a switch-on threshold voltage VT of the transistor (172; again, see Fig. 7D; also see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65).

11. As pertaining to **Claim 21**, Blalock discloses that the analogue DC voltage (150) representing the gray level applied to the storage capacitor (160) varies between 0 volts (i.e., 0V) and the same threshold voltage value VT (again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65 and note that this is a necessary driving condition in order for the circuit to function).

12. As pertaining to **Claim 22**, Blalock discloses that the liquid crystal cell (118) receives a supply voltage Vdd (i.e., any arbitrary voltage) for a fraction of a frame duration equal to Vi/VT or (VT-Vi)/VT (i.e., any arbitrary voltage and frame duration) and a zero voltage (i.e., 0V) the remainder of the time (see Fig. 8; also see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65).

13. As pertaining to **Claim 23**, Blalock discloses that a ramp generator (144; see Fig. 4A) is associated with each row of the matrix (102), a ramp beginning after an analogue voltage (i.e., an arbitrary analogue voltage) has been charged into a storage

capacitor (160) of each of the dots of the row (again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65).

14. As pertaining to **Claim 24**, Blalock discloses (see Fig. 8 and Fig. 7D) that two storage capacitors (160, 201) and two transistors (170, 172) are associated with each elementary liquid crystal cell (118), the first capacitor (160) and the first transistor (170) operating alternately with the second capacitor (201) and the second transistor (172) so as to store row by row an analogue voltage (150) representing a gray level in the first capacitor (160) during the even frames while the control of the cell (118) is effected by the second transistor (172) and the second capacitor (201), and so as to store row by row in the second capacitor (201) an analogue voltage (150) representing a gray level during the even frames while the control of the cell (118) is effected by the first transistor (170) and the second capacitor (160), the second terminal (162) of the first storage capacitor (160) being maintained at 0 volts (i.e., 0V) during the odd frames and receiving a linear ramp (see Fig. 7D) during the even frames, and conversely the second terminal (209) of the second capacitor (201) being maintained at 0 volts (i.e., 0V) during the even frames and receiving a linear ramp (see Fig. 7D) during the odd frames (again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65 and note that any arbitrary frame can be called an even frame and any arbitrary frame can be called an odd frame).

15. As pertaining to **Claim 25**, Blalock discloses (see Fig. 4A, Fig. 8, and Fig. 7D) a liquid crystal matrix display (102), including an active matrix (102) of image dots (i.e., pixels) and peripheral circuits (see Fig. 4A), the matrix (102) including a cross array of addressing lines (133) and of columns (131) for feeding in analogue voltages (150; see Fig. 8) representing the gray levels to be displayed on the dots (i.e., pixels) of each row and, for each dot (i.e., pixel) at the crossover of a row and of a column, an elementary electronic circuit (see Fig. 8) for controlling an elementary liquid crystal cell (118) situated at this crossover, the elementary circuit (see Fig. 8; also see Col. 1, Ln. 31-39; Col. 6, Ln. 38-60; and Col. 8, Ln. 11-46) comprising:

a storage capacitor (160) for storing for the duration of an image frame an analogue voltage (150) applied by the column, a first terminal (159) of the storage capacitor (160) being linked to the gate of the transistor (172; again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65),

in series between two voltage supply terminals (i.e., (V-) and (Illum, Bal, or V+), for example), an elementary current source (i.e., (170, 176, or 178), for example) and a switching transistor (i.e., any of (170, 176, 178)), the drain of the switching transistor (i.e., any of (170, 176, 178)) being linked to the liquid crystal cell (118; again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65),

the peripheral circuits (see Fig. 4) comprising an input for receiving a periodic voltage ramp (see (144)), common to all the cells (118) of at least one row, the ramp (see Fig. 7D) being applied to a second terminal (161) of the storage capacitor (160) of the cells (118) of this row (again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65).

16. As pertaining to **Claim 26**, Blalock discloses that the gate-source threshold voltage for switching on the transistor (172) is VT, the ramp has an amplitude of VT (see Fig. 7D), and the analogue voltage (150) representing the gray level can vary between 0 (i.e., 0V) and VT (again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65; and note that this is a necessary driving condition in order for the circuit to function).

17. As pertaining to **Claim 27**, Blalock discloses (see Fig. 8 and Fig. 7D) that the elementary circuit (see Fig. 8) associated with each image dot (i.e., pixel) is a circuit with double memory (i.e., two capacitors) comprising two storage capacitors (160, 201) and two switching transistors (170, 172) linked to the same elementary cell (118) and operating alternately one frame out of two, a voltage value being applied to a first capacitor (160) during an odd frame whereas the second capacitor (201) retains the voltage that it received during the previous even frame, and conversely, the circuit

comprising a disabling facility (i.e., signals or switches) for switching off the transistor (172) linked to the first capacitor (160) so as to disable the transistor (172) during the odd frame and a disabling facility (i.e., signals or switches) for switching off the transistor (170) linked to the second capacitor (201) so as to disable this transistor during the even frame (again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65 and note that any arbitrary frame can be called an even frame and any arbitrary frame can be called an odd frame).

18. As pertaining to **Claim 28**, Blalock discloses a ramp generator (144; see Fig. 4A) for applying a ramp (see Fig. 7D) to all the first capacitors (160) during the even frames and for applying a ramp (see Fig. 7D) to all the second capacitors (201) of the matrix during the odd frames (again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65 and note that any arbitrary frame can be called an even frame and any arbitrary frame can be called an odd frame).

19. As pertaining to **Claim 30**, Blalock discloses (see Fig. 8 and Fig. 7D) that the elementary circuit (see Fig. 8) associated with each image dot (i.e., pixel) is a circuit with simple memory (i.e., at least one capacitor) with a single storage capacitor (160) and a single switching transistor (172), and in that a ramp generator (144; see Fig. 4D) is provided for applying to the storage capacitors (160) of a row of dots (i.e., pixels) of

the matrix a ramp (see Fig. 7D) which starts after an operation of storage in the capacitors (160) of the cells (118) of this row and which lasts for the remainder of a frame duration, the operations of storing analogue voltages in the capacitors (160) being performed row by row (again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65).

20. As pertaining to **Claim 31**, Blalock discloses (see Fig. 7) that consecutive image frames are sequentially displayed, each frame corresponding to modulation of light of a respective color of a color image to be displayed by the matrix (again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65).

21. As pertaining to **Claim 32**, Blalock discloses (see Fig. 8 and Fig. 7D) that the elementary circuit (see Fig. 8) associated with each image dot (i.e., pixel) is a circuit with double memory (i.e., two capacitors) comprising two storage capacitors (160, 201) and two switching transistors (170, 172) linked to the same elementary cell (118) and operating alternately one frame out of two, a voltage value being applied to a first capacitor (160) during an odd frame whereas the second capacitor (201) retains the voltage that it received during the previous even frame, and conversely, the circuit comprising a disabling facility (i.e., signals or switches) for switching off the transistor (172) linked to the first capacitor (160) so as to disable the transistor (172) during the

odd frame and a disabling facility (i.e., signals or switches) for switching off the transistor (170) linked to the second capacitor (201) so as to disable this transistor during the even frame (again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65 and note that any arbitrary frame can be called an even frame and any arbitrary frame can be called an odd frame).

22. As pertaining to **Claim 33**, Blalock discloses a ramp generator (144; see Fig. 4A) for applying a ramp (see Fig. 7D) to all the first capacitors (160) during the even frames and for applying a ramp (see Fig. 7D) to all the second capacitors (201) of the matrix during the odd frames (again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65 and note that any arbitrary frame can be called an even frame and any arbitrary frame can be called an odd frame).

23. As pertaining to **Claim 34**, Blalock discloses (see Fig. 8 and Fig. 7D) that the elementary circuit (see Fig. 8) associated with each image dot (i.e., pixel) is a circuit with simple memory (i.e., at least one capacitor) with a single storage capacitor (160) and a single switching transistor (172), and in that a ramp generator (144; see Fig. 4D) is provided for applying to the storage capacitors (160) of a row of dots (i.e., pixels) of the matrix a ramp (see Fig. 7D) which starts after an operation of storage in the capacitors (160) of the cells (118) of this row and which lasts for the remainder of a

frame duration, the operations of storing analogue voltages in the capacitors (160) being performed row by row (again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65).

24. As pertaining to **Claim 35**, Blalock discloses (see Fig. 7) that consecutive image frames are sequentially displayed, each frame corresponding to modulation of light of a respective color of a color image to be displayed by the matrix (again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65).

25. As pertaining to **Claim 36**, Blalock discloses (see Fig. 7) that consecutive image frames are sequentially displayed, each frame corresponding to modulation of light of a respective color of a color image to be displayed by the matrix (again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65).

26. As pertaining to **Claim 37**, Blalock discloses (see Fig. 7) that consecutive image frames are sequentially displayed, each frame corresponding to modulation of light of a respective color of a color image to be displayed by the matrix (again, see Col. 20, Ln. 30-67 through Col. 21, Ln. 1-54 in conjunction with Col. 10, Ln. 65-67 through Col. 11, Ln. 1-67 along with Col. 13, Ln. 35-67 through Col. 14, Ln. 1-65).

Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON M. MANDEVILLE whose telephone number is 571-270-3136. The examiner can normally be reached on Monday through Friday 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander Eisen can be reached on 571-272-7687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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